eFuse Design and Reliability

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Abstract— Programmable eFuse designs present an integration challenge in modern CMOS processing. The power level to program a fuse, and the programming methodologies leverage reliability mechanisms which all other elements in a design avoid. A high degree of eFuse process control and circuit design is required in order to guarantee operation. Almost all eFuse types are one time programmable and are limited to "one chance" programmable. This paper will discuss selected eFuse technologies describing the design philosophy, electrical programming and characterization, the physics of failure, and some of the many applications an on chip programmable element provides.

The implementation of a reliable electronically programmed fuse (eFuse) [1-4], fig. 1, has been introduced in the 0.25µm node, and continues to be used in present day nodes. A typical eFuse design in the programmed state is shown in the Transmission Electron Micrograph (TEM) of figure 2. The eFuse is integrated within the standard technology elements. In this case the polycided eFuse is designed over an isolation region with cathode and anode connections to the back end of line wiring. The design takes advantage of enhanced joule heating by leveraging the thermal isolation below and above the eFuse. The wiring interconnects are also leveraged in that their electromigration (EM) resistance far exceeds the eFuse element.

Programmed eFuses are electrically high resistance, while unprogrammed eFuses remain in a low resistance state. Programming is accomplished by controlling EM of the fuse link from the anode to the cathode by one time CMOS activation. The original polysilicon grain structure and silicide in fig 2 is preserved in the cathode region, while joule heating accompanied with EM moves the silicide from the eFuse link. This feature is clearly shown by the absence of silicide in this cross section, and in comparing an un-programmed and programmed eFuse in fig 1. The cross section of fig 2 also indicates the permanent silicon recrystallization that takes place during programming between the anode and cathode terminals. A physical open, or high resistance circuit is formed in the vicinity of the anode, as well as dopant redistribution in the underlying polysilicon within the link. The result is a one time, or one chance program event that alters the fuse state from low to high resistance.

Figure 3 shows the unprogrammed resistance of the entire electrical network, which includes the eFuse and associated read sense logic. In order to properly discriminate between a programmed and unprogrammed eFuse, a sense latch must be properly positioned so that a false sense is disallowed. In this figure the latch trip position as well as the programmed resistance at time zero is shown. There are orders of magnitude difference between a programmed and unprogrammed eFuse. The program resistance is also measured at end of life using an accelerated 500 hours voltage and temperature condition. In addition to this reliability life test a temperature and humidity stress condition under the above mentioned acceleration conditions is also applied. The eFuse reliability of programmed and unprogrammed parts was demonstrated to be 100% [1]. In this work we noted programmed resistance values greater than ~1E10Ω are related to test resolution. eFuse programming is limited to "one chance", or a single attempt. If in programming the fuses of fig 2 one terminates the programming logic early so that the fuse resistance is between the unprogrammed and programmed values of fig 3 it becomes impossible to supplement programming as an intermediate eFuse resistance limits the current that subsequent CMOS program logic can deliver.

eFuse scaling through design and electrical programming is demonstrated by the scanning electron micrographs in figures 1 and 4. Figure 1 shows programmed and unprogrammed eFuses in a 0.25µm bulk silicon node and figure 4 shows eFuses a 90nm SOI scaled node. eFuse operation through controlled EM of a silicided region on a doped polysilicon link is thus a scaleable technology element, unlike a laser fuse in the back end metallurgy which remains at relatively constant dimensions.

The eFuse methodology will extend into future nodes. However, a high K gate insulator using a metal gate electrode may require additional innovation to deploy an eFuse. Reliability studies as performed in [1] will have to again be conducted. As shown in [4] redesign and additional optimization of the eFuse may ensue.

This element will remain pervasive through all levels of chip assembly

One field mitigation technique that may be employed through eFuse is an "e-exchange" of critical performance blocks that may wear out more quickly than others[5]. For example, autonomic replacement of an I/O can be realized with on chip eFuse. Product lifetimes can thus be significantly improved. eFuse may be the ultimate reliability switch that can be used to sustain products beyond a typical useful life.

Technology and ULSI require a fuse technology that will couple to geometric scaling. The density and quantity of replacement elements as well as their use in customizing a final end product continues to drive requirements for an eFuse device.

References:

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[3] C.Kothandaraman et al., "Electrically programmable fuse (eFUSE) using electromigration in silicides", IEEE EDL, V23 I9 p523 (2002)
[4] C. Tian et al., "Reliability Qualification of CoSi2 Electrical Fuse for 90Nm Technology", IEEE IRPS Proceedings p392 (2006)
[5] W. Tonti et al, "Digital reliability monitor having autonomic repair and notification capability" USPA7,287,177 (2007)

This work was performed at the IBM Microelectronics,Division Semiconductor Research & Development Center Hopewell Junction NY 12533, and in Essex Junction VT 05452

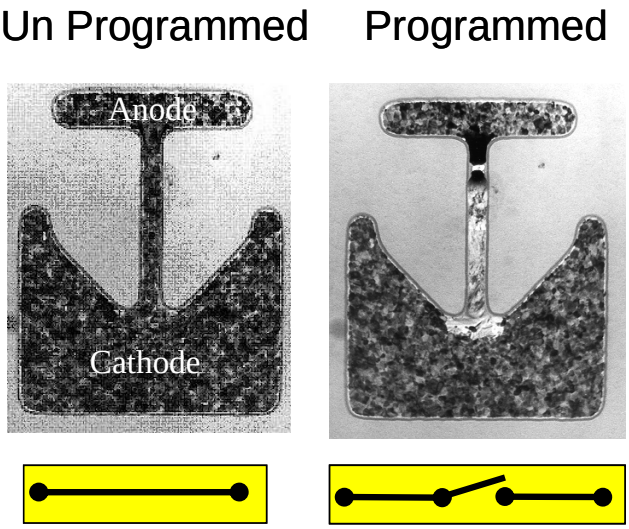

Figure 1: : eFuse in a 0.25µm Bulk Silicon node. Shown are programmed(right) and unprogrammed (left) eFuses. Programming is accomplished by silicide electromigration. The fuse link width between the cathode and anode terminals is 0.20µm

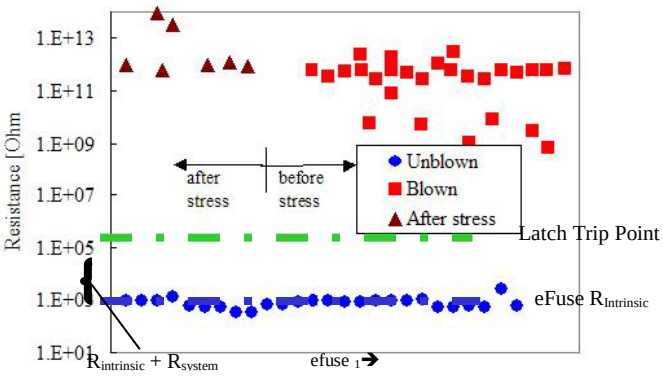

Figure 3: Nine order of magnitude delta between Unblown/Unprogrammed fuses, and Blow/Programmed fuses at a time zero measurement. Subsequent high voltage, high temperature 500 hour stress indicates no movement in fuse healing. Note resistances above 1E10 are at tester resolution limits. Practical consideration for a latch trip point is also show to provide margin.

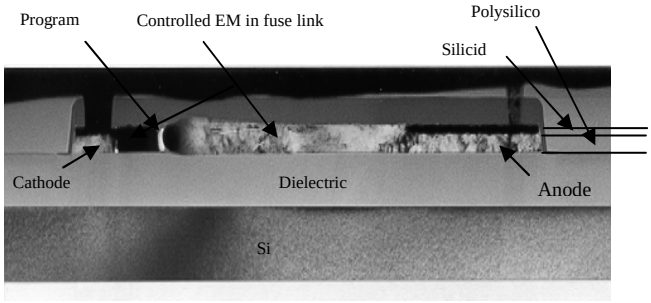

Figure 2: Cross section of programmed eFuse link in Fig. 19 showing polysilicon grain structure and original silicide structure in the anode. Controlled EM in the fuse link, recrystallization of the polysilicion, and programming of the fuse link is identified.

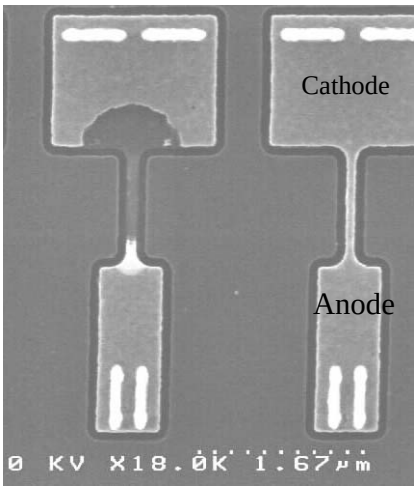

Figure 4: eFuse in a 90nm Silicon on Insulator node. Shown are programmed (left) and unprogrammed (right) eFuses. Programming is accomplished by silicide electromigration and dopant redistribution within the polysilicon link. The fuse link width between the cathode and anode terminals is 90nm.